IN THE CLAIMS:

Please cancel claims 23-27 and 29-32 as follows:

Claim 1. (original) Communication device for processing outgoing and incoming packets, the device comprising:

a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal;

a mode line connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive mode; and

a control line to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

Claim 2. (original) Communication device for processing an outgoing packet, the device comprising:

a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; and

a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the preceding signal processing units.

Claim 3. (original) Communication device for processing an incoming packet, the device comprising: aplurality of signal processing units connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal; and

a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the signal processing units following in the signal processing chain.

Claim 4. (original) Device according to claim 1, wherein each signal processing unit comprises a multiplexing unit.

Claim 5. (original) Device according to claim 2, wherein each signal processing unit comprises a multiplexing unit.

Claim 6. (original) Device according to claim 3, wherein each

signal processing unit comprises a multiplexing unit.

Claim 7. (original) Device according to claim 1, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

Claim 8. (original) Device according to claim 2, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

Claim 9. (original) Device according to claim 3, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output.

Claim 10. (original) Device according to claim 1, wherein each signal processing unit is connected via a logic unit to the control line.

Claim 11. (original) Device according to claim 2, wherein each signal processing unit is connected via a logic unit to the control line.

Claim 12. (original) Device according to claim 3, wherein each signal processing unit is connected via a logic unit to the control line.

Claim 13. (original) Device according to claim 10, wherein the logic unit comprises an OR gate.

Claim 14. (original) Device according to claim 11, wherein the logic unit comprises an OR gate.

Claim 15. (original) Device according to claim 12, wherein the logic unit comprises an OR gate.

Claim 16. (original) Device according to claim 1, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

Claim 17. (original) Device according to claim 2, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop

processing.

Claim 18. (original) Device according to claim 3, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

Claim 19. (original) Device according to claim 1, wherein each signal processing unit is usable for the transmit and receive mode.

Claim 20. (original) Transceiver unit comprising a transceiver controller and a communication device, both transceiver controller and communication device being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; a mode line connected to each processing unit for switching each processing unit between a transmit mode and a receive mode; and a control line to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

Claim 21. (original) Transceiver unit comprising a transceiver controller and a communication device, both being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; and a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the preceding signal processing units.

Claim 22. (original) Transceiver unit comprising a transceiver controller and a communication device, both being interconnected, the transceiver unit is adapted to communicate with a buffer unit via a bus system; wherein said communication device comprises: a plurality of signal processing units connected in sequence thereby forming a signal

processing chain, each signal processing unit being clocked by a common clock signal; and a control line to which each signal processing unit is connected, the control line communicating flow information to at least one of the signal processing units following the signal processing chain.

Claims 23-27. (canceled)

Claim 28. (original) Baseband system comprising a communication device, wherein said communication device comprises: a plurality of signal processing units connected in sequence, each signal processing unit being clocked by a common clock signal; a mode line connected to each processing unit for switching each processing unit between a transmit mode and a receive mode; and a control line to which each signal unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units.

Claims 29-32. (canceled)